AMENDMENTS TO SPECIFICATION

Please amend the paragraph beginning at page 1, line 12 as follows:

The present disclosed system relates to field-programmable gate arrays, and more particularly, to a freeway architecture for tileable field-programmable gate arrays. This application is a continuation in part of US patent application entitled "TILEABLE FIELD-PROGRAMMABLE GATE ARRAY ARCHITECTURE" serial number 09/654,240, filed on September 2, 2000 now issued patent number 6,476,636.

Please amend the paragraph beginning at page 15, line 7 as follows:

Each FG 40 also includes a CL input 47 and a CO output 45. The purpose of these input and output ports is to implement a carry chain for faster utilization of logic resources.

Please amend the paragraph beginning at page 35, line 17 as follows:

The full disclosures of the following copending U.S. patent applications are hereby incorporated into the present application by reference: U.S. Patent Application No. 09/231,998, filed January 15, 1999, entitled "STORAGE CELLS UTILIZING REDUCED PASS GATE VOLTAGES FOR READ AND WRITE OPERATIONS", and commonly assigned herewith; U.S. Patent Application No. 09/281,008, filed March 30, 1999, entitled "METHOD AND APPARATUS FOR INCREASING THE SPEED OF FIELD-PROGRAMMABLE GATE ARRAYS", and commonly assigned herewith; U.S. Patent Application No. 09/285,563, filed April 2, 1999, entitled "METHOD AND APPARATUS FOR STORING A VALIDATION NUMBER IN A FIELD-PROGRAMMABLE GATE ARRAY" now issued U.S. Patent Number 6,446,242, and commonly assigned herewith; and U.S. Patent Application No. 09/318,198, filed May 25,

1999 now issued U.S. Patent Number 6,211,697, entitled "INTEGRATED CIRCUIT THAT INCLUDES A FIELD-PROGRAMMABLE GATE ARRAY AND A HARD GATE ARRAY HAVING THE SAME UNDERLYING STRUCTURE", and commonly assigned herewith.

Please amend the Abstract of this invention beginning at page 49, line 2 as follows:

A freeway routing system for a field programmable gate array (FPGA)~~. The system~~ comprising a first FPGA tile. The first FPGA tile comprising a plurality of functional groups (FGs) arranged in rows and columns; a plurality of interface groups (IGs) surrounding the plurality of FGs such that one IG is positioned at each end of each row and column, each of the IGs having a first, second and third set of input ports and a first, second and third set of output ports[;]. A ~~a~~ freeway routine system including a set of routing conductors configured to transfer signals to said first, second and third input ports, and configured to transfer signals from said first, second and third output ports of IGs in different PEG/IO/RAM[;] ~~, said freeway~~ The set of routing conductors comprising: a plurality of vertical conductors that form intersections with a plurality of horizontal conductors; and programmable interconnect elements located at said intersections in a diagonal orientation on said FPGA tile. ~~It is emphasized that this abstract is provided to comply with the rules requiring an abstract that will allow a searcher or other reader to quickly ascertain the subject matter of the technical disclosure. It is submitted with the understand that it will not be used to interpret or limit the scope or meaning of the claims. 37 CFR 1.72(b).~~